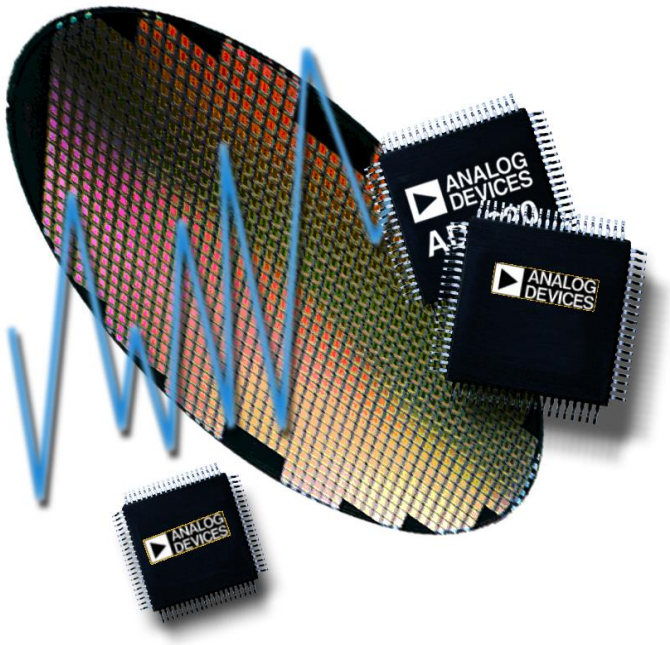

Reliability Report

Report Title: LTM4702 Material Set Change Qualification

Report Number: 21000

Revision: A

Date: 4 October 2023

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the LTM4702 product in a 49-CSP_BGA package. The LTM4702 is using 200um die thickness and Substron substrate.

Die/Fab Product Characteristics

Table 1: LTM4702 Product Characteristics

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data
Generic/Root Part #	LTM4702	LTM4702
Die Id	8625	8625
Die Size (mm)	1.57 x 1.77	1.57 x 1.77
Die Thickness (um)	200	450
Wafer Fabrication Site	Vanguard	Vanguard
Wafer Fabrication Process	0.35µm DMOS	0.35µm DMOS
Die Substrate	Si	Si
Metallization / # Layers	AlCu/ 3 Layers	AlCu/ 3 Layers
Polyimide	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN

Package/Assembly Product Characteristics

Table 2: LTM4702 Product Characteristics - 49-CSP_BGA at ADI Penang

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data
Generic/Root Part #	LTM4702	LTM4702
Package	49-CSP_BGA	49-CSP_BGA
Body Size (mm)	6.25 x 6.25 x 5.07	6.25 x 6.25 x 5.07
Assembly Location	ADPG	ADPG
MSL/Peak Reflow Temperature(°C)	4 / 250	4 / 250
Mold Compound	Sumitomo G311E	Sumitomo G311E
Substrate Material	BT Resin	BT Resin
Terminal Finish	96.5Sn_3.0Ag_0.5Cu	96.5Sn_3.0Ag_0.5Cu

QMCL

PID P/N	Description	Vendor, Vendor P/N
PMS0460PG01E03	6.25x6.25mm Substrate	Subtron, PMS0460PG01E03

Package/Assembly Test Results

Table 3: Package/Assembly Test Results - CSP_BGA at ADI Penang

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Sample Size	Qty Failures
Solder Heat Resistance (SHR)	J-STD-020	MSL-4	LTM4702	Q21000.1SHR	246	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 2,000 Hours	LTM4702	Q18656.1HTS	45	0
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125°C, Biased, 1,000 Hours	LTM4702	Q18656.1HTOL	77	0
				Q18661.1HTOL	77	0
				Q18661.3HTOL	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST)2	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264hrs	LTM4702	Q18661.1BHAST.REPLACE	25	0
				Q18661.2HAST	25	0
				Q18661.3HAST	25	0
Power Cycle	JESD22-A122	50,000 Cycles	LTM4702	Q18661.1PWRCYC	8	0
				Q18661.2PWRCYC	8	0
				Q18661.3PWRCYC	8	0
Temperature Cycling (TC)2	JESD22-A104	-55°C/+125°C, 1,000 Cycles	LTM4702	Q21000.1TC	77	0
		-55°C/+125°C, 2,000 Cycles		Q18656.1TC	77	0
		-65°C/+150°C, 2,000 Cycles		Q18661.1TC	77	0
				Q18661.2TC	77	0
Unbiased HAST (UHST)2	JESD22-A118	110C 85%RH 17.7 psia, 264hrs	LTM4702	Q18656.1UHAST	77	0
				Q18661.1UHAST	77	0
				Q18661.2UHAST	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 4) prior to the start of the stress test. Level 4 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 96 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 245°C.

ESD and Latch-Up Test Results

Table 4: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class
JESD78	LTM4702	+100mA, -100mA	+19.5V/+4.9V	25°C	I

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	LTM4702	49-CSP_BGA	JS-002	1Ω, Cpkg	±1250V	C3
HBM	LTM4702	49-CSP_BGA	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	3A

Approvals

Reliability Engineer: Lay Yong Ong